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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,317	10/20/2003	Hyun T. Kim	2003-0551.00/US	4522

26809 7590 03/21/2007

MICRON TECHNOLOGY, INC.
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EXAMINER	
BARNES, SETH W	
ART UNIT	**PAPER NUMBER**
2822	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/690,317	KIM ET AL.	
	Examiner	Art Unit	
	Seth Barnes	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments and Amendments

Applicant's arguments and amendments filed 12 September 2007 have been fully considered but they are not persuasive.

Regarding **claims 19** and **21** rejected under 35 U.S.C. §103(a) as being unpatentable over Park et al. (U.S. 5,296,400) in view of Ravi et al. (U.S. 6,548,313), the Applicant states on page 4, "Ravi et al. does not teach that the planarized amorphous carbon filler is a continuous layer residing between and abutting to the adjacent transistor gate structures as presently claimed in the instant invention (see Fig. 4 and 5A)." The Applicant further states on page 5, "There is no indication that the teachings of Park et al. and Ravi et al. are combinable and even if they are combinable, the combination thereof would not result in a 'planarized amorphous carbon filler that is a continuous layer residing between and abutting to the adjacent transistor gate structures' as presently claimed in the instant invention, but instead might result in a planarized amorphous carbon filler that is 'not' a continuous layer residing between and abutting to adjacent gate structures as Fig. 4 and 5A of Ravi et al. demonstrates."

The Examiner respectfully disagrees. In Fig. 4 (shown below) the planarized amorphous carbon filler (**404, 402**) is a continuous layer residing between and abutting to the adjacent transistor gate structures. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to

produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Park et al. reference by including the amorphous carbon filler material and the planarizing step as taught by Ravi et al. in order to facilitate the etching process and to improve etch selectivity (Ravi et al., col. 3, lines 1-6).

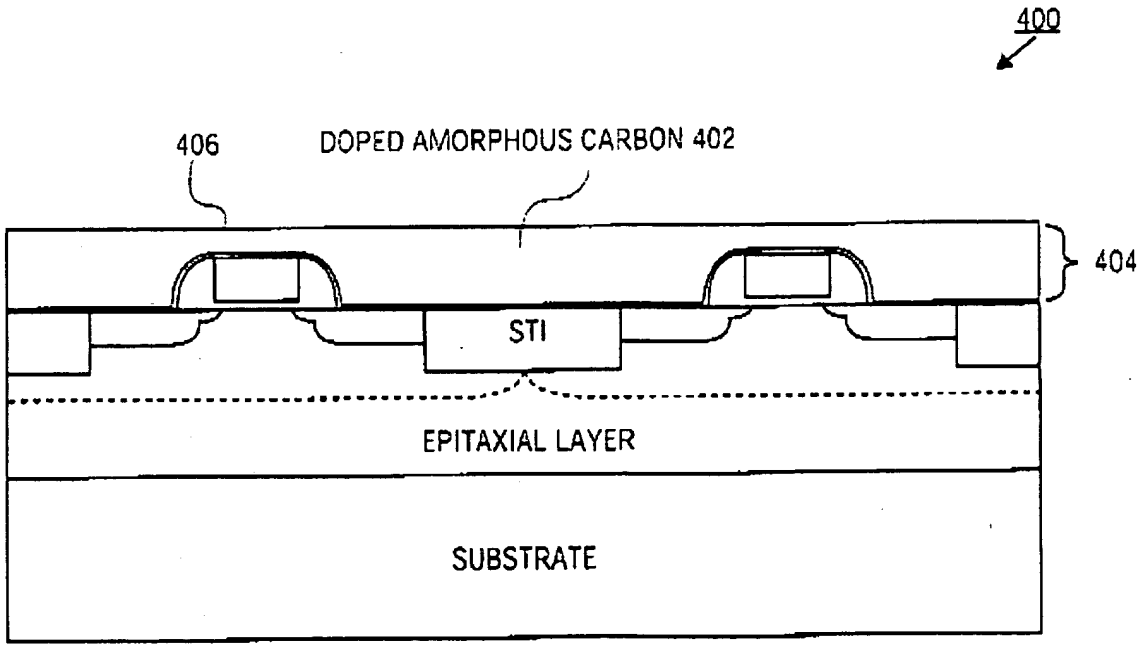

FIG. 4

Regarding **claim 21** rejected under 35 U.S.C. §103(a) as being unpatentable over Wei et al. (U.S. 6,423,645) in view of Ravi et al. (U.S. 6,548,313), the Applicant states on page 6, "Ravi et al. does not teach that the planarized amorphous carbon filler is a continuous layer residing between and abutting to the adjacent transistor gate structures as presently claimed in the instant invention (see Fig. 4 and 5A)." The Applicant further states on pages 6 and 7, "There is no indication that the teachings of Wei et al. and Ravi et al. are combinable and even if they are combinable, the combination thereof would not result in a 'planarized amorphous carbon filler that is a continuous layer residing between and abutting to the adjacent transistor gate structures' as presently claimed in the instant invention, but instead might result in a planarized amorphous carbon filler that is 'not' a continuous layer residing between and abutting to adjacent gate structures as Fig. 4 and 5A of Ravi et al. demonstrates.

The Examiner respectfully disagrees. In Fig. 4 (shown above) the planarized amorphous carbon filler (**404, 402**) is a continuous layer residing between and abutting to the adjacent transistor gate structures. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to a person of

ordinary skill in the art at the time of the invention to modify Wei et al. reference by including the planarizing step as taught by Ravi et al. in order to facilitate the etching process (col. 3, lines 1-6).

Regarding **claim 20** rejected under 35 U.S.C. §103(a) as being unpatentable over Park et al. (U.S. 5,296,400) in view Ha (U.S. 6,451,708) and Ravi et al. (U.S. 6,548,313), the Applicant states on page 8, "Ravi et al. does not teach that the planarized amorphous carbon filler is a continuous layer residing between and abutting to the adjacent transistor gate structures as presently claimed in the instant invention (see Fig. 4 and 5A)." The Applicant further states on page 8, "There is no indication that the teachings of Park et al., Ha and Ravi et al. are combinable and even if they are combinable, the combination thereof would not result in a 'planarized amorphous carbon filler that is a continuous layer residing between and abutting to the adjacent transistor gate structures' as presently claimed in the instant invention, but instead might result in a planarized amorphous carbon filler that is 'not' a continuous layer residing between and abutting to adjacent gate structures as Fig. 4 and 5A of Ravi et al. demonstrates."

The Examiner respectfully disagrees. In Fig. 4 (shown above) the planarized amorphous carbon filler (**404, 402**) is a continuous layer residing between and abutting to the adjacent transistor gate structures. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to

produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Park et al. reference by including the amorphous carbon filler material and the planarizing step as taught by Ravi et al. in order to facilitate the etching process and to improve etch selectivity (Ravi et al., col. 3, lines 1-6) and to specify the aspect ratio being greater than about 5:1 as taught by Ha in order to obtain a high aspect ratio contact holes concurrently in the cell array a region and the peripheral circuit region without increasing the process steps and the cost (Ha, col. 2, lines 45-67).

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 19 and **21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. (US 5,296,400) in view of Ravi et al. (US 6,548,313). Park et al. shows a method of fabricating a transistor source/drain connection between adjacent transistor gate structures (Abstract). Park et al. discloses depositing a filler material at least in a region between the adjacent transistor gate structures (Fig. 2B). Park et al. teaches

removing the filler material with a process having removal selectivity to nitride greater than 40:1 to form a contact opening and depositing a conductive material (polysilicon) in the contact opening (Fig. 2D-2F, col. 4, lines 10-25, col. 52-65). Park et al. shows the filler material being a continuous layer (Fig. 2B-2D). Park et al. does not specifically show depositing and planarizing an amorphous carbon filler material. However, Ravi et al. teaches depositing and planarizing the amorphous carbon filler material between adjacent transistor gate structures as well known in the art (Fig. 4-5A, 9B, col. 2, lines 60-65, col. 3, lines 1-6, 24-60). Ravi et al. shows the amorphous carbon filler material being a continuous layer that is planarized before being etched (Fig. 4, col. 3, lines 1-6, 24-60, col. 4, lines 50-60). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Park et al. reference by including the amorphous carbon filler material and the planarizing step as taught by Ravi et al. in order to facilitate the etching process and to improve etch selectivity (Ravi et al., col. 3, lines 1-6).

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wei et al. (US 6,423,645) in view of Ravi et al. (US 6,548,313). Wei et al. shows a method of fabricating a transistor source/drain connection between adjacent transistor gate structures (col. 3, lines 50-60). Wei et al. discloses depositing an amorphous carbon filler material at least in a region between the adjacent transistor gate structures (col. 3, lines 8-17, col. 4, lines 27-35). Wei et al. teaches selectively dry developing the carbon filler material to form a contact opening and depositing a polysilicon material in the

contact opening (Abstract, Fig. 7, col. 1, lines 5- 20, col. 3, lines 60-67, col. 4, lines 27-35). Wei et al. does not specifically show planarizing the amorphous carbon filler material such that the planarized amorphous carbon filler material remains only between the adjacent transistor gate structures. However, Ravi et al. teaches planarizing the amorphous carbon filler material such that the planarized amorphous carbon filler material remains only between the adjacent transistor gate structures (Fig. 4-5A, 9B, col. 2, lines 60-65, col. 3, lines 1-6, 24-60). Ravi et al. shows the amorphous carbon filler material being a continuous layer that is planarized before being etched (Fig. 4, col. 3, lines 1-6, 24-60, col. 4, lines 50-60). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Wei et al. reference by including the planarizing step as taught by Ravi et al. in order to facilitate the etching process (col. 3, lines 1-6).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. (US 5,296,400) in view of Ha (U.S. 6,451,708) and Ravi et al. (US 6,548,313). Park et al. shows a method of fabricating a transistor source/drain connection between adjacent transistor gate structures (Abstract). Park et al. discloses depositing a filler material at least in a region between the adjacent transistor gate structures (Fig. 2B). Park et al. teaches removing the filler material with a process having removal selectivity to nitride greater than 40:1 to form a contact opening and depositing a conductive material in the contact opening (Fig. 2D-2F, col. 4, lines 10-25, col. 52-65).

Park et al. does not specifically show depositing and planarizing an amorphous carbon filler material. However, Ravi et al. teaches depositing and planarizing the amorphous carbon filler material between adjacent transistor gate structures as well known in the art (Fig. 4-5A, 9B, col. 2, lines 60-65, col. 3, lines 1-6, 24-60). Ravi et al. shows the amorphous carbon filler material being a continuous layer that is planarized before being etched (Fig. 4, col. 3, lines 1-6, 24-60, col. 4, lines 50-60). Park et al. does not specifically show the aspect ratio being greater than about 5:1. However, Ha shows forming a contact opening having the aspect ratio greater than about 5:1 (col. 6, lines 40-65). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Park et al. reference by including the amorphous carbon filler material and the planarizing step as taught by Ravi et al. in order to facilitate the etching process and to improve etch selectivity (Ravi et al., col. 3, lines 1-6) and to specify the aspect ratio being greater than about 5:1 as taught by Ha in order to obtain a high aspect ratio contact holes concurrently in the cell array a region and the peripheral circuit region without increasing the process steps and the cost (Ha, col. 2, lines 45-67).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lim et al. (US 6,380,106) (of record) is cited as evidence to show that the use of amorphous carbon as a filler material is conventional in the art.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seth Barnes whose telephone number is (571) 272-6008. The examiner can normally be reached on Monday thru Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Zandra V. Smith
Supervisory Patent Examiner
12 March 2007

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SWB

03/08/07

Zandra V. Smith
Supervisory Patent Examiner
12 March 2007